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<b>TO:</b>	Examiner E. Lee GAU 2815	<b>PHONE #:</b>	(703) 305-5695
<b>FROM:</b>	Mark Zagorin	<b>DATE:</b>	January 30, 2003
<b>SUBJECT:</b>	Response to non-final Office action		
<b>YOUR REF:</b>	09/484,311	<b>OUR REF:</b>	1001-0087
<b>FACSIMILE #:</b>	(703) 308-7722	<b>PAGES:</b>	6 (including this transmittal)

**MESSAGE**

Please see attached

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

#13/Response

2/3/03

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Applicant(s): James John Casto et al.

Title: INTEGRATED CIRCUIT PACKAGE INCORPORATING  
PROGRAMMABLE ELEMENTS

Application No.: 09/484,311

Filed: January 18, 2000

JAN 30 2003

Examiner: E. Lee

Group Art Unit: 2815

TECHNOLOGY CENTER 2800

Atty. Docket No.: 1001-0087

January 30, 2003

COMMISSIONER FOR PATENTS  
Washington, DC 20231

**RESPONSE TO NON-FINAL OFFICE ACTION**

This paper is responsive to a Non-Final Office Action dated October 30, 2002, having a shortened statutory period for response set to expire January 30, 2003.

REMARKS

Claims 2-12, 15-25, and 27 are pending in the application.

Claims 2-5, 10, 11, 17, 18, 22, and 23 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,369,437 B1 to MacPherson et al. MacPherson fails to teach a package comprising at least one one-time programmable element having a first and a second end separated by a programmable link. In the Office Action dated October 30, 2002, the Examiner states that "[t]he whole semiconductor device may be construed as a 'package.' For example, a semiconductor device such as a PAL, FPGA or PLD which contain fuses may be called a package or any substrate (i.e. circuit board) it is put on may be called a package." The Examiner relies on col. 1, line 46-col. 2, line 32 of MacPherson to support this statement. Applicants respectfully submit that the Examiner has misinterpreted the reference. MacPherson teaches at col. 1, lines 46-51 that PALs, FPGAs, and PLDs are fabricated and programmed after they are packaged units. However, MacPherson distinguishes between a device and a package and fails